4.20.1 – Standard Template for JEDEC Module Standards

Standard Template for JEDEC Module Standards

The following material describes a list of items which are required in order to fully describe industry standard module designs. This is a requirement for industry standard modules as frequency and complexity of design and compatibility requirements increase. Currently there is no restriction as to the amount of information which must be included in order to fully describe new modules.

Comprehensive standards must include most or all of the data defined in the attached sections, only removing items when they are not applicable. (This template is intended to act as a basis for creating module standards, and the sponsor must decide which of the contents are appropriate for a particular module design).

This template is based on the existing JEDEC-standard 168 Pin PC133 DIMMs, 184 Pin DIMMs, and 200 Pin DDR SODIMMs, and has been extracted from these ballots.

In order to submit a module for standardization/publication in JEDEC, the following comprehensive contents must be documented as listed below. In the case where some sections do not apply to the proposed module, this must be indicated in place of the described contents. If the sponsor feels certain sections are not necessary to define the key attributes, this should also be defined prior to balloting.

1. Overview
    - -Product Description
    - -DIMM Organization
    - -DIMM Dimensions
    - -Pin Count
    - -SDRAMs supported
    - -DIMM capacity supported
    - -Serial PD
    - -Voltage Options
    - -Interface
    - -Raw Card Summary
    - -Intended Market
    - -Product Family Summary
    - -Product types (Non-parity, ECC, Registered, Reg/Buf, Unbuffered etc)
        - -Compatibility
    - -Similar pin rotations to prior standards
    - -Similar dimensions to prior standards

2. Application Environment (for reference only)
    - -Typical Operating environment
        - -Temperature
        - -Humidity
        - -Forced/convection airflow
        - -Altitude
        - -Operating voltages/tolerances

3. Architecture
    - -DIMM Pinout Summary (# pins of each type)
    - -DIMM Pin Definitions
    - -DIMM Pin Assignments
    - -DIMM Block Diagrams
    - -Logical Clock Structures
    - -Functional Assignments of support components

4. Component Details (reference to other JEDEC standards is preferred):
    - -DRAM Component Specifications
        - -Pin assignments
        - -Pkg info
        - -DC Electrical Characteristics

-AC Timing Parameters
-Support Chip Component Specifications (if applicable)
-Pinouts
-Pkg info
-Component use on the DIMM
-Key device functions/attributes (if new and/or not generally known)
-Key device timings (or reference applicable JEDEC standards/ballots)
-Reference generic (JEDEC standard) device P/Ns (if applicable)

5. Card Details:
-Raw Card types/configurations expected/proposed
-Describe expected/proposed matrix of mainstream raw card options expected
-Assign names if 'reference' Gerber files to be included as part of standard
-Definition of SDRAM organizations/addressing supported on each card
-Input Loading Matrix
-Include all input loads seen by the system
-Design File Revision Matrix (if 'reference' designs planned)
-Proposed or 'reference' component placement (conceptual, unless 'reference' designs planned)

6. Card Wiring Details (Net Structure data):
-List Signal Groups described
-General Net Structure Routing Guidelines
-Net Structure Example (if necessary)
-Detailed wiring, termination and padding caps for each signal group to be shown
-Initially, a net structure (only) will be shown - no trace lengths
-Cross-section recommendations
-Electrical specifications
-Layer stack-ups

7. Timing Budget
-Timing Example
-Description of Timing Methodology

8. Serial PD Definition Example
-Describe the bytes that apply (based on the most recent JEDEC standard)
-Reference the JEDEC Serial PD Standard
-Provide example of most common DIMM type(s)

9. Product Label
-Dimensions/attributes (reference JC-11 if appropriate)
-Label contents and decode matrix

10. Detailed DIMM mechanical dimensions nominal example (reference to JC-11 standard required)
    -Describe any new and/or unique attributes
    -Connector type(s) expected

11. Supporting Hardware General Description (if applicable)
    -Clock Reference Board
    -Any other applicable hardware associated with this module family

12. Application Notes (if applicable)
    -Background/usage of new features
        (- For example: Power-on reset modes, new pins such as 'ZZ' pin, PLL input inactivity detection, CKE forcing methods,..)
    -Serial PD usage/new features
    -Clock Tuning Methodology
    -Clock Reference Board Operation/features

13. Revision Log