# JEDEC STANDARD

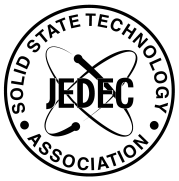
## Ball Grid Array Pinouts Standardized for 32-Bit Logic Functions

## JESD75

**NOVEMBER 1999**

**ELECTRONIC INDUSTRIES ALLIANCE**

**JEDEC Solid State Technology Association**




## NOTICE

EIA/JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the EIA General Counsel.

EIA/JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

EIA/JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the EIA/JEDEC standards or publications.

The information included in EIA/JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby an EIA/JEDEC standard or publication may be further processed and ultimately become an ANSI/EIA standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this EIA/JEDEC standard or publication should be addressed to JEDEC Solid State Technology Association, 2500 Wilson Boulevard, Arlington, VA 22201-3834, (703)907-7560/7559 or www.jedec.org

Published by
©ELECTRONIC INDUSTRIES ALLIANCE 1999
2500 Wilson Boulevard
Arlington, VA 22201-3834



**PRICE: Please refer to the current**
**Catalog of JEDEC Engineering Standards and Publications or call Global Engineering Documents, USA and Canada (1-800-854-7179), International (303-397-7956)**

PLEASE!

DON"T VIOLATE
THE
LAW!



JEDEC Solid State Technology Association
2500 Wilson Boulevard
Arlington, Virginia 22201-3834
or call (703) 907-7559

# BALL GRID ARRAY PINOUTS STANDARDIZED FOR 32-BIT LOGIC FUNCTIONS

**(Formerly JEDEC Board Ballot JCB-99-51, formulated under the cognizance of the JC-40 Committee on Digital Logic.)**

## 1 Background

### 1.1 Purpose

To provide a pinout standard for dual-die 32-bit logic devices offered in a 96- and 114-ball grid array package for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

### 1.2 Scope

This standard defines device pinout for 32-bit wide buffer, driver and transceiver functions. This pinout specifically applies to the conversion of DIP-packaged 16-bit logic devices to LFBGA-packaged dual-die 32-bit logic devices.

## 2 Definitions for the purpose of this document

### 2.1 Definitions

DIP: Dual In-line Pin Package (gull-wing)

LFBGA: Low-Profile Fine-Pitch Ball Grid Array (MO-205)

SSOP: Shrink Small-Outline Package; 0.25" lead pitch; 0.3" wide body (MO-118)

TSSOP: Thin Shrink Small-Outline Package; 0.5-mm lead pitch; 6.4-mm wide body (MO-153)

TVSOP: Thin Very Small-Outline Package; 0.4-mm lead pitch; 4.4-mm wide body (MO-194)

## 3 Pinout standard

### 3.1 Description

The following criteria shall be used to convert existing 16-bit logic device functions offered in 48- and 56-pin DIP packages (SSOP, TSSOP, TVSOP) to 32-bit logic device functions offered in 96- and 114-ball LFBGA packages:

A. Attributes for the LFBGA packages shall be as follows:

(1) 96-Ball, 0.8-mm ball pitch with 5.5-mm × 13.5-mm body size and 6-row × 16-column ball matrix, or the

(2) 114-Ball, 0.8-mm ball pitch with 5.5-mm × 16.0-mm body size and 6-row × 19-column ball matrix.

B. Device conversion shall be as follows:

| DIP package | LFBGA package |
|---|---|
| 48-pin | 96-ball |
| 56-pin | 114-ball |

C. The pinout conversions shall be in accordance with the diagrams shown in section 3.3 and 3.6.

### 3.2 96-ball LFBGA (MO-205CC)

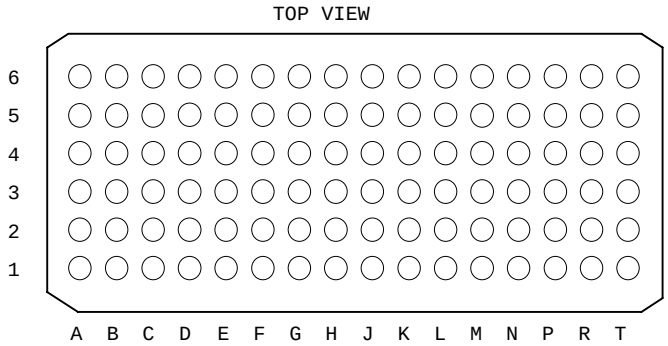



**Figure 1. Pinout configuration**

### 3.3 Pin conversion for 96-ball LFBGA

The pin conversion adopts the naming convention of logic devices in 48-pin packages (e.g. SSOP, TSSOP, TVSOP).

| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 6 | A46¶ | A43¶ | A40¶ | A37¶ | A35¶ | A32¶ | A29¶ | A27¶ | B46¶ | B43¶ | B40¶ | B37¶ | B35¶ | B32¶ | B29¶ | B27¶ |
| 5 | A47¶ | A44¶ | A41¶ | A38¶ | A36¶ | A33¶ | A30¶ | A26¶ | B47¶ | B44¶ | B41¶ | B38¶ | B36¶ | B33¶ | B30¶ | B26¶ |
| 4 | A48§ | A45† | A42‡ | A39† | A34† | A31‡ | A28† | A25§ | B48§ | B45† | B42‡ | B39† | B34† | B31‡ | B28† | B25§ |
| 3 | A1§ | A4† | A7‡ | A10† | A15† | A18‡ | A21† | A24§ | B1§ | B4† | B7‡ | B10† | B15† | B18‡ | B21† | B24§ |
| 2 | A2¶ | A5¶ | A8¶ | A11¶ | A13¶ | A16¶ | A19¶ | A23¶ | B2¶ | B5¶ | B8¶ | B11¶ | B13¶ | B16¶ | B19¶ | B23¶ |
| 1 | A3¶ | A6¶ | A9¶ | A12¶ | A14¶ | A17¶ | A20¶ | A22¶ | B3¶ | B6¶ | B9¶ | B12¶ | B14¶ | B17¶ | B20¶ | B22¶ |

**Figure 2. Pin conversion top view**

### 3.4 Pin assignment for 96-ball LFBGA

†GND: B3, B4, D3, D4, E3, E4, G3, G4, K3, K4, M3, M4, N3, N4, R3, and R4

‡$V_{DD}$: C3, C4, F3, F4, L3, L4, P3, and P4

§Control: A3, A4, H3, H4, J3, J4, T3, and T4

¶I/O and Signals: all Row-1, -2, -5 and -6 pins.

### 3.5 114-ball LFBGA (MO-205DC)

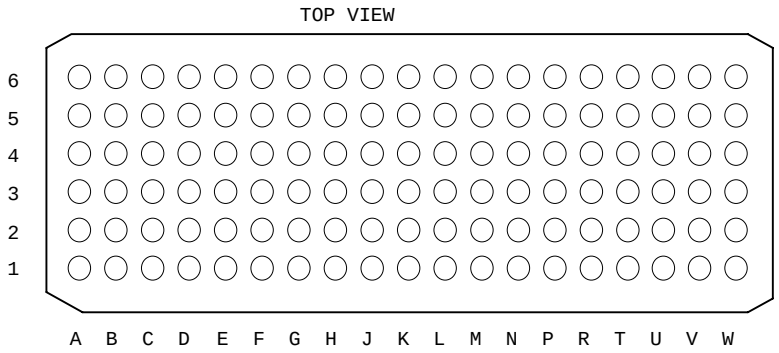



**Figure 3. Pinout configuration**

### 3.6 3.6 Pin conversion for 114-ball LFBGA

The pin conversion adopts the naming convention of logic devices in 56-pin packages (e.g. SSOP, TSSOP, TVSOP).

| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T | U | V | W |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 6 | A52# | A49# | A47# | A44# | A42# | A40# | A37# | A36# | A33# | NC* | B52# | B49# | B47# | B44# | B42# | B40# | B37# | B36# | B33# |
| 5 | A54§ | A51# | A48# | A45# | A43# | A41# | A38# | A34# | A31§ | B55§ | B54§ | B51# | B48# | B45# | B43# | B41# | B38# | B34# | B31§ |
| 4 | A55§ | A56¶ | A53† | A50‡ | A46† | A39† | A35‡ | A32† | A30§ | A29¶ | B56¶ | B53† | B50‡ | B46† | B39† | B35‡ | B32† | B30§ | B29¶ |
| 3 | A2§ | A1§ | A4† | A7‡ | A11† | A18† | A22‡ | A25† | A27§ | A28§ | B1§ | B4† | B7‡ | B11† | B18† | B22‡ | B25† | B27§ | B28§ |
| 2 | A3§ | A6# | A9# | A12# | A14# | A16# | A19# | A23# | A26§ | B2§ | B3§ | B6# | B9# | B12# | B14# | B16# | B19# | B23# | B26§ |
| 1 | A5# | A8# | A10# | A13# | A15# | A17# | A20# | A21# | A24# | NC* | B5# | B8# | B10# | B13# | B15# | B17# | B20# | B21# | B24# |

**Figure 4. Pin conversion top view**

†GND Pins: C3, C4, E3, E4, F3, F4, H3, H4, M3, M4, P3, P4, R3, R4, U3, and U4

‡$V_{DD}$ Pins: D3, D4, G3, G4, N3, N4, T3, and T4

§Control Pins: A2, A3, A4, A5, B3, J2, J3, J4, J5, K2, K3, K5, L2, L3, L5, V3, V4, W2, W3, and W5

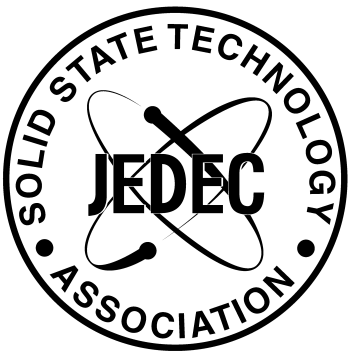
¶GND or Control Pins: B4, K4, L4, and W4

#I/O Pins: A1, A6, B1, B2, B5, B6, C1, C2, C5, C6, D1, D2, D5, D6, E1, E2 ,E5 ,E6, F1, F2, F5, F6, G1, G2, G5, G6, H1, H2, H5, H6, J1, J6, L1, L6, M1, M2, M5, M6, N1, N2, N5, N6, P1, P2, P5, P6, R1, R2, R5, R6, T1, T2, T5, T6, U1, U2, U5, U6, V1, V2, V5, V6, W1, and W6

*No Connection Pins: K1 and K6

## 4 Reference to other applicable JEDEC standards and publications

JEP95: *JEDEC Registered and Standard Outlines for Solid State and Related Products*


SOLID STATE TECHNOLOGY
JEDEC
ASSOCIATION